Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

All claims currently being amended are shown with deleted text struckthrough or double bracketed and new text underlined. Additionally, the status of each claim is indicated in parenthetical expression following the claim number.

Claims 1 - 21 remain.

Claims 1, 3, 5, 7 – 9, 12, 14 and 17 are being amended.

Claims 2, 4, 11 and 13 are being cancelled.

WHAT IS CLAIMED IS:

1. (Currently Amended) A method of performing digital to analog conversion comprising:

generating a pulse width modulated data stream and another pulse width modulated data stream including generating encoding patterns of the pulse width modulated data stream by selectively generating early and late pattern edges relative to edges of a reference such that the encoding patterns of the pulse width modulated data stream [[selected to]] minimize distortion in the another pulse width modulated stream caused by edges in the pulse width modulated data stream, and wherein selectively generating early and late pattern edges comprises:

tracking a number of early and late edges generated in previously generated encoding patterns; and

selectively generating a late or early edge in at least one subsequent encoding pattern such that an average number of early edges in the pulse width modulated data stream approximates an average number of late edges in the pulse width modulated data stream;

converting in corresponding digital to analog conversion elements the

pulse width modulated data stream and the another pulse width modulated data stream into an analog signal and another analog signal; and

summing the analog signal and the another analog signal to generate an output signal.

2. (Cancelled)

3. (Currently Amended) The method of Claim 1 [[2]], wherein selectively generating early and late pattern edges comprises selectively varying right and left pattern edges in the encoding patterns relative to corresponding left and right edges in the reference pattern.

4. (Cancelled)

5. (Currently Amended) [[The method of Claim 2,]] A method of performing digital to analog conversion comprising:

generating a pulse width modulated data stream and another pulse width modulated data stream including generating encoding patterns of the pulse width modulated data stream by selectively generating early and late pattern edges relative to edges of a reference pattern such that the encoding patterns of the pulse width modulated data stream minimize distortion in the another pulse width modulated stream caused by edges in the pulse width modulated data stream, wherein selectively generating early and late pattern edges comprises:

varying a count in a counter from a neutral count value in response to a late or early edge in selected encoding patterns generated; and

generating a late or early edge in a subsequent encoding pattern which varies the count in the counter towards the neutral count value;

converting in corresponding digital to analog conversion elements the pulse width modulated data stream and the another pulse width modulated data stream into

an analog signal and another analog signal; and

summing the analog signal and the another analog signal to generate an output signal.

6. (Original) The method of Claim 1, wherein generating the pulse width modulated data stream and the another pulse width modulated data stream comprises generating first and second pulse width modulated data streams together encoding a single input stream.

7. (Currently Amended) [[The method of Claim 2,]] A method of performing digital to analog conversion comprising:

generating a pulse width modulated data stream and another pulse width modulated data stream including generating encoding patterns of the pulse width modulated data stream by selectively generating early and late pattern edges relative to edges of a reference pattern such that the encoding patterns of the pulse width modulated data stream minimize distortion in the another pulse width modulated stream caused by edges in the pulse width modulated data stream, wherein a number of early pattern edges is approximately equal to a number of late pattern edges generated in the pulse width modulated data stream;

converting in corresponding digital to analog conversion elements the pulse width modulated data stream and the another pulse width modulated data stream into an analog signal and another analog signal; and

summing the analog signal and the another analog signal to generate an output signal.

8. (Currently Amended) [[The method of Claim 2,]] A method of performing digital to analog conversion comprising:

generating a pulse width modulated data stream and another pulse width modulated data stream including generating encoding patterns of the pulse width modulated data stream by selectively generating early and late pattern edges relative to edges of a reference pattern such that the encoding patterns of the pulse width modulated data stream minimize distortion in the another pulse width modulated stream caused by edges in the pulse width modulated data stream, wherein a number of late pattern edges substantially exceeds a number of early pattern edges generated in the pulse width modulated data stream;

converting in corresponding digital to analog conversion elements the pulse width modulated data stream and the another pulse width modulated data stream into an analog signal and another analog signal; and

summing the analog signal and the another analog signal to generate an output signal.

9. (Currently Amended) A digital to analog conversion system comprising:

pulse width modulation circuitry for generating first and second pulse width modulated data streams, encoding patterns of the first pulse width modulated data stream selected to minimize distortion in the second pulse width modulated stream caused by edges in the first pulse width modulated data stream and wherein the pulse width modulation circuitry generates the encoding patterns of the first data stream by generating early and late pattern edges relative to edges of a reference pattern and is operable to:

track a number of early and late edges generated in previously generated encoding patterns in the first pulse width modulated data stream; and

selectively generate a late or early edge in at least one subsequent encoding pattern in the first pulse width modulated data stream such that an average number of early edges approximates an average number of late edges;

first and second digital to analog conversion elements for respectively converting the first and second the first and second analog signals to generate the analog output signal.

10. (Original) The digital to analog conversion system of Claim 9, wherein the pulse width modulation circuitry comprises a ternary pulse width modulation stage.

11. (Cancelled)

12. (Currently Amended) The digital to analog conversion system of Claim 9 [[11]], the pulse width modulation circuitry generates early and late pattern edges by selectively varying right and left pattern edges in the encoding patterns relative to corresponding left and right edges in the reference pattern.

13. (Cancelled)

14. (Currently Amended) [[The digital to analog converter of Claim 11,]] A digital to analog conversion system comprising:

pulse width modulation circuitry for generating first and second pulse width modulated data streams, encoding patterns of the first pulse width modulated data stream selected to minimize distortion in the second pulse width modulated stream caused by edges in the first pulse width modulated data stream and wherein the pulse width modulation circuitry generates the encoding patterns of the first data stream by generating early and late pattern edges relative to edges of a reference pattern and [[wherein the pulse width modulation circuitry]] comprises:

a counter counting from a neutral count value in response to a late or early edge in selected encoding patterns generated in the first pulse width modulated stream; and

circuitry causing generation of a late or early edge in a subsequent encoding pattern which varies the count in the counter towards the neutral count

value; and

first and second digital to analog conversion elements for respectively converting the first and second the first and second analog signals to generate the analog output signal.

15. (Original) The digital to analog converter of Claim 14, wherein the neutral count value is zero, the counter increments by a selected value in response to an early edge and decrements by the selected amount in response to an late edge.

16. (Original) The digital to analog converter of Claim 9, wherein the first and second digital to analog conversion elements comprise continuous-time digital to analog conversion elements.

17. (Currently Amended) An digital to analog conversion system comprising:

a noise shaper for requantizing a digital input data stream;

pulse width modulation circuitry for generating first and second pulse width modulated data streams in response to the output of the noise shaper, encoding patterns of the first pulse width modulated data stream selected to minimize distortion in the second pulse width modulated stream caused by edges in the first pulse width modulated data stream, and wherein the pulse width modulation circuitry generates the encoding patterns of the first data stream by generating early and late pattern edges relative to edges of a reference pattern and is operable to:

track a number of early and late edges generated in previously generated encoding patterns in the first pulse width modulated data stream; and

selectively generate a late or early edge in at least one subsequent encoding pattern in the first pulse width modulated data stream such that an average number of early edges approximates an average number of late edges;

and

first and second digital to analog conversion elements for respectively converting the first and second pulse width modulated data streams into first and second analog signals; and

an analog summer for summing the first and second analog signals to generate the analog output signal.

18. (Original) The digital to analog conversion system of Claim 17, wherein the pulse width modulation circuitry comprises a first encoder for generating the first pulse width modulated data stream and a second encoder for generating the second pulse width modulated data stream, the first and second encoders encoding an input stream from the noise shaper such that first and second pulse width modulated streams together encode the input stream.

19. (Original) The digital to analog conversion system of Claim 17, wherein the first and second encoders operate respectively on first and second input streams output from the noise shaper.

20. (Original) The digital to analog conversion system of Claim 19, further comprising deinterleaving circuitry for switching the first and second input streams output from the noise shaper respectively to the first and second encoders.

21. (Original) The digital to analog conversion system of Claim 17, wherein the first and second digital to analog conversion elements comprises elements of a digital filter.